WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, the method comprising:

forming a storage layer over a semiconductor body, the storage layer including a first boundary layer, an intermediate storage layer and a second boundary layer;

patterning the storage layer so that at least some of the storage layer is removed from over a first portion of the semiconductor body and some of the storage layer is removed from over a second portion of the semiconductor body;

doping the first portion of the semiconductor body; and

etching the second portion of the semiconductor body without etching the first portion of the semiconductor body.

2. The method of claim 1 wherein the first boundary layer comprises an oxide layer, wherein the storage layer comprises a nitride layer, and wherein the second boundary layer comprises an oxide layer.

3. The method of claim 1 wherein patterning the storage layer comprises:

forming a mask over the storage layer;

forming openings in the mask over the first portion of the semiconductor body and over the second portion of the semiconductor body; and

etching portions of the storage layer that are exposed by the openings.

4. The method of claim 3 wherein etching the second portion of the semiconductor body comprises:

forming a second mask over the storage layer; and

forming an opening in the second mask over the second portion of the semiconductor body.

5. The method of claim 4 wherein the opening in the second mask is larger than the opening in the mask over the second portion, and wherein the etching is performed using the storage layer as an etch mask.

6. The method of claim 3 wherein doping the first portion of the semiconductor body comprises implanting ions through the openings in the mask.

7. The method of claim 1 and further comprising doping the second portion of the semiconductor body at the same time the first portion is doped.

8. The method of claim 1 and further comprising forming an auxiliary layer over the storage layer prior to patterning the storage layer.

9. The method of claim 8 wherein the auxiliary layer comprises at least one material selected from the group consisting of polysilicon, nitride, and oxide.

10. The method of claim 1 wherein the semiconductor body comprises a semiconductor substrate.

11. A method for fabricating semiconductor memories with charge trapping memory cells, the method comprising:

in a first step, applying a storage layer sequence made of dielectric material to a semiconductor body, the layer sequence comprising a first boundary layer, a storage layer and a second boundary layer;

in a second step, forming buried bit lines in the semiconductor body by introducing dopants through a mask with openings; and

in a third step, completing formation of a memory device,

wherein:

in the second step, the mask is provided with at least one further opening for the definition of an alignment mark and the material of the storage layer is removed in the region of the openings and of each further opening; and

in a further step between the second and third steps, using a further mask, a cutout is etched out into the semiconductor body in the region of an alignment mark to be fabricated.

12. The method of claim 11 and further comprising:

in a second further step between the first and second steps, applying an auxiliary layer to the second boundary layer;

wherein:

in the second step, the auxiliary layer is removed in the region of the openings and of each further opening; and

after the further step, the auxiliary layer is removed.

13. The method of claim 12 wherein the auxiliary layer comprises a polysilicon layer.

14. The method of claim 11 wherein the semiconductor body comprises a semiconductor substrate.

15. A method for forming an alignment mark while fabricating a semiconductor memory with charge trapping memory cells, the method comprising:

providing a silicon body;

forming a storage layer over the semiconductor body by forming a first oxide layer followed by forming a nitride layer followed by forming a second oxide layer;

forming a first masking layer over the storage layer;

forming a first opening in the masking layer over a first portion of the silicon body and a second opening in the masking layer of a second portion of the silicon body;

removing portions of the second oxide layer and the nitride layer exposed by the first opening and the second opening;

forming a buried bitline by doping the first portion of the silicon body;

removing the first masking layer;

forming a second masking layer over the storage layer;

forming an opening in the second masking layer over the second portion of the masking layer; and

etching the second portion of the silicon body.

16. The method of claim 15 wherein forming an opening in the second masking layer comprises forming an opening that is larger than the second opening, wherein the second portion of the silicon body is etched using the storage layer as an etch mask.

17. The method of claim 16 and further comprising removing a portion of the first oxide layer exposed by the opening in the second masking prior to etching the second portion of the silicon body.

18. The method of claim 17 wherein removing a portion of the first oxide layer further includes removing a portion of the second oxide layer, and wherein the second portion of the silicon body is etched using the nitride layer as an etch mask.

19. The method of claim 15 and further comprising forming an auxiliary layer over the storage layer prior to forming the first masking layer.

20. The method of claim 20 wherein the auxiliary layer comprises a polysilicon layer.